Pokhara University
Faculty of Science and Technology

Course No.: CMP 262 — Full marks: 100

Course title: **Computer Architecture (3-1-1)** — Pass marks: 45

Nature of the course: Theory & Practical — Total Lectures: 45 hrs

Level: Bachelor — Program: BE (Computer)

1. Course Description

This course is designed to provide the knowledge of the evolution of computer architecture and the factors influencing the design of hardware and software elements of computer systems. It aims to provide an understanding of the design of processing unit and control unit architectures. This course introduces the concepts of instruction set design, processor processor organization, pipelining, cache and virtual memory organizations, I/O and interrupts, parallel processing and multicore computers.

2. General Objectives

- To acquaint the students with the knowledge of computer architecture and associated processing, control unit and ALU unit of very simple central processing unit.
- To provide the knowledge of the functions of each element of memory hierarchy.
- To develop the skills in students to choose the appropriate Memory and Input Output organization used in real world computing systems.
- To acquaint the students with the knowledge of technology behind modern advanced computer architectures for parallel processing and multicore architecture.

3. Methods of instructions

Lectures, Tutorials, Case Studies, Discussion, Readings and Practical Works.

4. Content in details

Specific objectives	Contents
● Understand the concepts of computer architectures, functional units and components of computer systems and various addressing modes.	**Unit 1 Introduction to Architecture [4 Hrs]** 1.1.Brief overview of Computer organization and Architecture 1.2.Hierarchy structure of computer system 1.3. Computer evolution and generations 1.4. Computer Components and Functions 1.5. Future Trends in Computer 1.6. Review of Instruction sets, Addressing Modes and Instruction format

• Understand the VHDL Programming for simple operations.	**Unit -2: Register Transfer Language and Micro operations [4Hrs]** 2.1 Register Transfer and RTL 2.2.Micro Operation 2.3 Data Transfer Micro Operations 2.4 Arithmetic and Logical Operations 2.5 Shift Micro operations 2.6 Introduction to HDL and VHDL 2.7 VHDL programming for Adder, Mux, ALU
• Understand the functional units of CPU and their organization.	**Unit -3: Processor Organization [5 Hrs]** 3.1CPU Organization/Structure 3.2 Register Organization and Data paths 3.3 Instruction Cycle(T states) 3.4 Arithmetic and Logical Unit 3.5 Design Principles for Modern Systems
• Understand the design of Hardwired and microprogrammed control units.	**UNIT 4 Control Unit [5 Hrs]** 4.1 Control of the processor 4.2 Hardwired Control Unit(Control unit inputs/logic) 4.3 Microinstruction Format 4.4 Micro Programmed Control Unit 4.5 Architecture of Microprogrammed Control Unit 4.6 Microinstruction Sequencing and Execution 4.7 Application of Hardwired and Micro programmed Control Units 4.8 RISC and CISC Architecture
• Understand the representation of binary numbers in signed and unsigned notation along with the algorithms used for the basic arithmetic operations.	**UNIT 5 Computer Arithmetic [7 Hrs.]** 5.1 Integer Representation 5.2 Integer Arithmetic 5.3 Unsigned Binary Addition and Subtraction 5.4 Unsigned Binary Multiplication Algorithm 5.5 Booth Multiplication Algorithm 5.6 Unsigned Binary Division Algorithm 5.7 Floating Point Representation
• Understand the concepts of pipelining for better performance.	**Unit 6: Pipelining [4 hrs]** 6.1 Pipelining 6.2 Arithmetic Pipeline 6.3 Instruction Pipeline 6.4 Conflicts in Instruction Pipelining and their solutions 6.5 RISC pipeline 6.6 Register Windowing and Register Renaming
• Review memory Hierarchy of computer systems and understand the principles of cache memory to increase the performance of CPU	**UNIT 7 Memory Organization [4 Hrs.]** 7.1 Memory Hierarchy 7.2 Main Memory and Auxiliary Memory 7.3 Associative Memory and Cache Memory 7.4 Cache mapping techniques- Direct,Associative

	and Set Associative Mapping 7.5 Cache Write Policy. 7.6 Cache Replacement algorithm (FIFO, LRU, LFU)
• Familiarize with IO interfaces and introduce various methods for improving I/O performances.	**Unit 8: Input-Output Processing [4 Hrs]** 8.1 Peripheral Devices 8.2 I/O Modules 8.3 I/O Interface and Techniques 8.4 Modes of Transfer: Programmed,Interrupt-Driven and DMA 8.5 I/O Processor and IO channel 8.6 GPU and TPU 8.7 External Interfaces: FireWire and Infiniband 244
• Understand the concept of parallel processing and multi thread architecture in modern processors.	**Unit 9: Parallel \Processing [4 Hrs]** 9.1 Parallel Processing 9.2 Parallelism In Uniprocessor system 9.3 Multiprocessor System and their characteristics 9.4 Flynn Classification 9.5 Interconnection structures in Multiprocessors 9.6 Vector processing and Array processing 9.7 Introduction to Multithreaded Architecture
• Prevalent new development in computer architecture: the use of multiple processors on a single chip	**Unit 10:Multi-core computer (4Hrs)** 10.1 Hardware performance issues 10.2 Software Performance Issues 10.3 Multicore Organization 10.4 Dual Core, Quad Core and Octa Core 10.5 Power Efficient Processor

5. Laboratory Works

Laboratory works of 15 hours per group of maximum 24 students should cover the following lab works:.

1. Write a program to implement the Booth Algorithm (2hr)
2. Write a program to implement the Non Restoring Division Algorithm (2 hr)
3. Write a VHDL Code for Realizing Logic Gates (1hr)
4. Write a VHDL code for Combination circuits (Decoder, Encoder, MUX, Demux ,Comparerator, Code converter) (6 Hrs)
5. Write a VHDL Program for Realizing Sequential Circuits Like Fliflop and counters (4 Hrs)

6. List of Tutorials:

The various tutorial activities that outfit this course should cover all the content of this course to give students a space to engage more actively with the course content in the presence of

the instructor. Students should submit tutorials as assignments or class works to the instructor for evaluation. The following tutorial activities of 15 hrs should be conducted to cover all the content of this course:

A. Discussion based Tutorials (3 hrs)

1. Overview of Computer Organization and Architecture.
2. Memory hierarchy for modern processors.
3. Comparative analysis of different aspects of computing systems as defined in Flynn's Classification.

B. Problem Solving based Tutorials (6 hrs)

1. Design a CPU for any given registers set, instruction set and state diagram.
2. Develop a control unit for any given state diagram.
3. Design a microsequencer control unit for any given specifications following design procedure.
4. Perform arithmetic addition and subtraction in signed and unsigned notation for any given numbers.
5. Perform Multiplication operation for any given numbers using shift-add multiplication algorithm and Booth's algorithm.
6. Perform Division operation for any given numbers using restoring and Non restoring Division algorithm.

C. **Review and Question/Answer-based Tutorials:** (6 hrs)

1. Case study on any of multi threaded and Multi core processors. It should include the architecture of processor, control unit, memory as well as input output organization in detail. An oral presentation with the submission of a report should be a part of work and must be included as a component for evaluation.
2. Students ask questions within the course content and assignments and review key course content in preparation for tests or exams.

7. Evaluation system and Students' Responsibilities

Evaluation:

Internal Evaluation	Weight	Marks	External Evaluation	Marks
Theory		30		
Attendance and class Participation	10%			
Assignments	20%			
Project work/Presentations	20%			
Term Exam	50%			
Practical		20		

Attendance and Lab Participation	20%		Semester End examination	50
Lab report	30%			
Practical Exam	30%			
Viva	20%			
Total Internal Marks		50		
Full marks=50+50				

Students Responsibility:

Each student must secure at least 45% marks separately in internal assessment and practical evaluation with 80% attendance in the class in order to appear in the semester End Examination. Failing to get such a score will be given NOT QUALIFIED(NQ) to appear for the Semester End Examination. Students are advised to attend all the classes, formal exam, test and complete all the assignments within the specified time period. Students are required to complete all the requirements defined for the completion of the course.

8. Prescribed Text Books and References

Text Books:

1. Stalling W. (2011). *Computer Organization and Architecture*, Pearson Education.

References:

2. Carpinelli, John D. (2001). *Computer System Organization and Architecture*. Pearson Education Asia.
3. Hall, Douglas V. (2005). *Microprocessor and Interfacing programming and Hardware*. McGraw Hill, New Delhi.
4. Tanenbaum, A.S. (2003). *Structured Computer Organization*. Pearson Education.
5. Uffenbeck, J. (1991). *Microcomputers and microprocessors: the 8080, 8085, and Z-80 programming, interfacing, and troubleshooting*. Prentice-Hall, Inc..
6. Moris M. M. (1992). *Computer System Architecture*. Pearson